Abstract of the Disclosure

A jitter detecting circuit and a phase locked loop using the detected jitter are provided. A jitter detecting circuit detecting a jitter value of a signal which is converted into a digital signal from an analog signal input, wherein the jitter value detecting circuit includes an edge detector discriminating signs of two signals derived from continuous sampling points from the digitally converted input signal, and outputting the two signals as first and second edge signals, respectively if the signs s are different from each other; a comparator outputting a signal having a smaller absolute value among the first and second edge signals output from the edge detector; an operating unit dividing the absolute value output from the comparator by the sum of the absolute value of the first edge signal and that of the second edge signal; and an accumulator accumulating outputs of the operating unit during a predetermined period, to obtain a jitter value of the predetermined period. A jitter amount is detected with signals derived from two sampling points around the edge from the analog-digital converted signal, so that an accurate jitter amount can be detected regardless of the input signal amplitude, and an accurate and fast phase locked signal can be obtained using the jitter value.